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(54) CIRCUITS FOR SUPPLYING ELECTRICAL CURRENT FROM AN  
ALTERNATING VOLTAGE SOURCE TO A LOAD

(71) We, MULLARD LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a circuit for supplying electrical current from an alternating voltage source to a load, including a semiconductor switch for connection in series with the load such that current is supplied to the load via the switch while the switch is on, a trigger current generator for supplying trigger current to the switch to turn on the switch, and control means for turning on and off the trigger current generator.

One example in the field of application of such a circuit is where the load is an electric motor, whereby controlling the switch controls the speeds of the motor to drive, for example, the drum of a washing machine.

A known circuit of the type described in the opening paragraph is disclosed in the Mullard Technical Handbook, Book one, Part seven, March 1975, on sheet TCA 280A page 7. The circuit shown includes a triac in series with a load and is designed for full wave a.c. phase control, i.e. for a given value of d.c. control voltage the triac should conduct for a corresponding proportion of each half cycle of the mains supply. A mains supply zero crossing detector together with a resistor-capacitor network provides a ramp waveform voltage in synchronism with and at double the frequency of the mains supply to one input of a difference amplifier. A d.c. control voltage is applied to the other input of the difference amplifier. For the portion of each half cycle of the mains supply for which the ramp waveform level exceeds the control voltage, the difference amplifier supplies a current to a further resistor-capacitor network causing a ramp function generator to operate and produce a burst of pulses whose width and repetition rate is dependent on the values of the re-

sistor and the capacitor in said further network. In the circuit disclosed the pulse width is 15  $\mu$ s and the repetition rate is such as to provide a maximum of 30 pulses per half cycle of the mains. Each pulse of the burst is applied to an output amplifier which provides a current pulse of the same width, and of an amplitude of 250 mA, to the trigger electrode of the triac.

In normal operation of the above circuit with a resistive load, the triac will be turned on by the first one of each burst of trigger pulses and the remaining pulses of that burst will be redundant. A disadvantage of the circuit resides in the high total current consumption of the circuit in providing these redundant trigger pulses. If the load is inductive, the current through the triac and the load will lag the mains supply voltage by a portion of each half cycle of the mains which is called the load phase angle. The first portion of each half cycle of the mains supply before the burst of trigger pulses commences is called the trigger angle. If the load phase angle is less than the trigger angle, then the triac will be turned on by the first one of each burst of trigger pulses as with a resistive load. If the load phase angle is greater than the trigger angle, then the first one of each burst of trigger pulses will not turn on the triac since it has not yet turned off. However, the next trigger pulse of the burst which occurs after the triac has turned off will turn it on again. This has the advantage of avoiding unidirectional conduction by the triac, but the trigger pulses of the burst before and after the one which is effective to turn it on will again be redundant. If, with either a resistive or an inductive load, the triac is inadvertently turned off by an interruption of the series connection of the triac and the load with the mains supply, then the first trigger pulse which occurs after that series connection is restored will turn on the triac again. This has the advantage of reducing the power which would otherwise be lost to the load as a result of such an interruption, but trigger

pulses other than the first trigger pulse which occurs after the series connection is restored are again redundant.

5 An object of the invention is to provide a circuit which has the same advantages as the above-described known circuit in that when used with a triac for phase control of an inductive load unidirectional conduction of the triac is avoided and the power lost to  
10 the load as a result of an interruption of the series connection of the triac and the load with the mains supply is reduced, but which does not have the disadvantage of a high total current consumption associated with the provision of redundant trigger pulses.

15 According to the invention there is provided a circuit for supplying electrical current from an alternating voltage source to a load, including a semiconductor switch for connection in series with the load such that  
20 current is supplied to the load via the switch while the switch is on, a trigger current generator for supplying trigger current to the switch to turn on the switch, and control means for turning on and off the trigger current generator, characterised in that the control means includes comparator means for comparing two control voltages, detection means responsive to the voltage across  
25 the switch, said detection means being adapted to provide a first detection signal if the voltage across the switch is larger in amplitude than a first predetermined value which is near zero volts but large enough such that if the switch is off it will hold on if  
30 it is then turned on, said detection means also being adapted to provide a second detection signal if the voltage across the switch is smaller in amplitude than a second predetermined value which is also near zero volts and furthermore is small enough to indicate that the switch has been substantially  
35 turned on when it had previously been off, and means interconnecting the comparator means and the detection means such that, in normal operation, during those periods of time when a first one of said control voltages is above a second one of said control voltages the control means is responsive to the first and  
40 second detection signals to respectively turn on and turn off the trigger current generator.

45 The basic idea of the invention is that if the comparator of two control voltages is used to determine periods of time during which is desired that the semiconductor switch should be on, then detection of the voltage across the semiconductor switch is alone sufficient to determine both when trigger current pulses occur within those periods  
50 of time and also the width of those trigger pulses.

55 In the case of a triac used for full wave phase control, the first one of said control

voltages will be above the second one of said control voltages for a given portion of each half cycle of the alternating voltage source. For an inductive load with the load phase angle substantially less than the trigger angle  
70 the triac will be off at the beginning of that portion of the half cycle and the voltage across the triac will be larger than said first predetermined value. Said first detection signal will therefore be immediately provided to turn on the trigger current generator. As soon as the triac is substantially on, the second detection signal will be provided to turn off the trigger current generator. A typical trigger current pulse having  
75 an amplitude of 200 mA has a width of 2  $\mu$ s or less. In normal operation no further trigger current pulses will be provided until the beginning of the appropriate portion of the next half cycle of the alternating voltage source. For an inductive load with the load phase angle greater than the trigger angle the triac will be on at the beginning of that portion of the half cycle of the alternating voltage source for which the first control voltage is above the second control voltage. The voltage across the triac will be smaller than said first predetermined value and so the trigger current generator will remain turned off. At the end of the load phase angle the current in the triac will reduce to zero and the triac will turn off. The voltage across the triac will then begin to rise and when it is greater than said first predetermined value the trigger current generator will be turned on. As soon as the triac is on, the trigger current generator will be turned off. In normal operation no further trigger current pulses will be provided until the end of the load phase angle in the next half cycle of the alternating voltage source. It will now be appreciated that if, whatever the relationship between the load phase angle and the trigger angle, the triac is inadvertently turned off by an interruption of the series connection of the triac and the load with the mains supply and this series connection is restored while the first control voltage is still above the second control voltage, then a single trigger current pulse will  
80 be provided to turn the triac on again substantially immediately after the restoration of the series connection.

85 As will be explained in more detail later, the invention does not only provide for the phase control of inductive loads via triacs. Within the scope of the invention circuits can be provided for phase control (otherwise known as conduction angle control) or burst firing control (otherwise known as time-proportional control) or static (on-off) switch control of resistive loads or inductive loads or capacitive loads via triacs or thyristors.

120 An embodiment of the invention will now

be described in detail with reference to the accompanying drawings, in which:—

Figure 1 shows a mainly schematic circuit diagram of a circuit for supplying electrical current from an alternating voltage source to a load, according to the invention, and a load connected to that circuit,

Figures 2 and 3 show waveforms which illustrate the operation of the circuit of Figure 1 when the load is purely resistive,

Figures 4 and 5 show waveforms which illustrate the operation of the circuit of Figure 1 when the load is inductive,

Figure 6 shows the detail of a ramp generator circuit which is part of the circuit of Figure 1,

Figure 7 shows voltage waveforms associated with Figure 6,

Figure 8 shows the detail of a voltage comparator which is part of the circuit of Figure 1,

Figure 9 shows the detail of detection means responsive to the voltage across the semiconductor switch, which means and switch are part of the circuit of Figure 1, and

Figure 10 shows the detail of a rectified voltage supply circuit, including means for detecting when the voltage supply is below a predetermined value, and a trigger current generator which form part of the circuit of Figure 1.

Referring now to Figure 1, a semiconductor switch in the form of a triac T is connected in series with a load L between the neutral terminal 1 and the line terminal 2 of an alternating voltage source, for example 240 volts r.m.s. at 50 Hz, such that current is supplied from the alternating voltage source to the load L while the triac T is on. The cathode of the triac T is connected directly to the neutral terminal 1 and the anode of the triac T is connected to the load L, which may be resistive, inductive or capacitive. The triac T is turned on by trigger current supplied to its gate electrode from a trigger current generator I1. Control means for turning on and off the trigger current generator I1 include a comparator COMP for comparing a first control voltage  $V_C$  and a second control voltage  $V_R$ , and detection means DET responsive to the voltage across the triac T. The control voltage  $V_C$  is a variable d.c. reference voltage derived from a potentiometer  $R_C$  and the control voltage  $V_R$  is a ramp waveform at double the frequency of the alternating voltage source from a ramp waveform generator 100, whereby for a given value of the voltage  $V_C$  that voltage is above the voltage  $V_R$  for a given portion of each half cycle of the alternating voltage source. A supply circuit 200 provides from the alternating voltage source a rectified voltage supply  $-V$  of a predetermined normal magnitude for normal

operation of the circuit. The supply circuit 200 includes low supply voltage detection means for providing an output signal which disables a NAND gate G1 if the magnitude of the voltage supply  $-V$  is less than a predetermined value which is substantially less than said normal magnitude. When the output signal of the supply circuit 200 disables the gate G1, the output of the gate G1 disables the comparator COMP so that it cannot turn on the current generator I1. However, in normal operation of the circuit when the gate G1 is enabled it gates a first detection signal from the detection means DET to enable the comparator COMP and it gates a second detection signal from the detection means DET to disable the comparator COMP. Thus, in normal operation of the circuit during that portion of the half cycle of the alternating voltage source when the voltage  $V_C$  is above the voltage  $V_R$ , the output of the comparator COMP turns the trigger current generator I1 on and off when it is respectively enabled and disabled by the output of the gate G1 in response to the output of the detection means DET. The first detection signal to enable the comparator COMP is provided by the detection means DET if the voltage across the triac T is larger in amplitude than a first predetermined value which is near zero volts but large enough such that if the triac T is off it will hold on if it is then turned on. The second detection signal to disable the comparator COMP is provided by the detection means DET if the voltage across the triac T is smaller in amplitude than a second predetermined value which is also near zero volts and furthermore is small enough to indicate that the triac T has been turned on when it had previously been off. These first and second predetermined values of the voltage across the triac T may conveniently coincide at a typical value of 20 volts.

The operation of the circuit of Figure 1 is illustrated for the case where the load L is purely resistive by the waveforms of Figures 2 and 3.

Referring to Figure 2A, the control voltages  $V_C$  and  $V_R$ , pulses of trigger current  $I_G$  supplied by the current generator I1 to the triac T, the voltage  $V_T$  across the triac T and the voltage  $V_L$  across the resistive load L are shown as waveforms on the same time scale as the voltage  $V_S$  of the alternating voltage source. The rising portion of the ramp voltage waveform  $V_R$  occurs during a short time before and after each zero crossing of the source voltage  $V_S$ . A very short pulse of trigger current  $I_G$  turns on the triac at the times t1, t2 and t3 which are at the beginning of the portion of each half cycle of the source voltage  $V_S$  for which the voltage  $V_C$  is above the voltage  $V_R$ . An extra pulse of trigger current  $I_G$  also occurs at the

time  $t_4$  in response to a temporary interruption of the series connection of the triac and the load with the source of voltage  $V_s$ . Since the load  $L$  is resistive, the current through the triac  $T$  and the load  $L$  are in phase with the voltage  $V_s$ . Thus at the time  $t_0$ , the reduction of the voltage  $V_s$  to zero reduces the current through the triac  $T$  and the load  $L$  to zero and the triac turns off. Between the times  $t_0$  and  $t_1$ , the triac is off, that is to say it is in its high impedance condition, such that the voltage  $V_T$  across the triac is substantially the voltage  $V_s$  whereas the voltage  $V_L$  across the load is substantially zero. At the time  $t_1$  the triac is turned on, that is to say it is changed to its low impedance condition, such that between the time  $t_1$  and the next zero crossing of the voltage  $V_s$  current is supplied from the source of voltage  $V_s$  to the load  $L$  via the triac with the voltage  $V_T$  across the triac being substantially zero and the voltage  $V_L$  across the load being substantially the voltage  $V_s$ . The triac  $T$  is on for the same portions of the succeeding two half cycles of the voltage  $V_s$ , being turned on by the pulses of trigger current  $I_G$  at the times  $t_2$  and  $t_3$ . At the time  $t_4$  there is a temporary interruption of the series connection of the triac and the load with the source of voltage  $V_s$ . At this time an extra pulse of trigger current  $I_G$  occurs, associated with this extra trigger pulse there is a temporary rise of the voltage  $V_T$  across the triac to just above the level at which the detection means DET is responsive, and the voltage  $V_L$  across the load temporarily drops to substantially zero volts.

Figure 2B shows the waveforms of Figure 2A at the time  $t_1$  on an expanded time scale wherein the width of the pulse of trigger current  $I_G$  occupies the time between the instants  $t_{10}$  and  $t_{12}$ . At the instant  $t_{10}$  the ramp voltage waveform  $V_R$  goes below the control voltage  $V_C$ . The voltage across the triac  $V_T$  is above the value  $V_D$  which is the coincident first and second values to which detector DET is responsive and so the comparator COMP is enabled by the gate G1 and turns on the trigger current generator I1 to initiate the pulse of trigger current  $I_G$ . We have found that when a triac is off there is a minimum value of voltage across the triac which must be present for the triac to hold on if it is then turned on by a trigger current pulse. This minimum voltage value is typically 2—5 volts with a resistive load of 1.2kW and a  $V_s$  of 240 volts r.m.s. The voltage level  $V_D$  to which the detector DET is responsive is set at a value which is well above that minimum value but very near zero volts in comparison with the value of the source voltage  $V_s$  for substantially the whole of each half cycle of the source voltage. With an alternating sinusoidal source

voltage of 240 volts r.m.s. at 50Hz having a peak value of 340 volts, a typical value of  $V_D$  which is suitable for the operation of the circuit of Figure 1 is 20 volts. From the instant  $t_{10}$  to the instant  $t_{11}$  while trigger current  $I_G$  is supplied to the triac the triac remains off, the voltage  $V_T$  across it continues to follow the voltage  $V_s$  and the voltage across the load  $V_L$  remains substantially zero. At the instant  $t_{11}$  the triac begins to turn on, the voltage  $V_T$  begins to fall and the voltage  $V_L$  begins to rise. At the instant  $t_{12}$  the voltage  $V_T$  becomes less than the value  $V_D$  and so the comparator COMP is disabled by the gate G1 and turns off the trigger current generator I1 to terminate the pulse of trigger current  $I_G$ . At the instant  $t_{13}$  the triac has turned on, the voltage  $V_T$  is substantially zero, in fact at a typical very small value one volt associated with its low impedance in the on state, and the voltage across the load  $V_L$  is substantially the source voltage  $V_s$ . The value  $V_D$ , typically 20 volts, is higher than the voltage across the triac when it has turned on at the time  $t_{13}$  but it is also near zero volts in comparison with the 340 volts peak value of the voltage  $V_s$  and is small enough to indicate that the triac has been substantially turned on when it had previously been off, such that the pulse of trigger current  $I_G$  can be terminated at the time  $t_{12}$ . A given triac will require a certain minimum value of trigger current to be applied to its gate electrode in order to turn on; furthermore the trigger current at whatever value above that minimum value will have to be applied for a minimum time such that a total charge is applied to the gate electrode which is sufficient to turn the triac on; and still furthermore the triac will take a certain time to respond to that applied charge before it turns on. For the Mullard triac type BT139 which has a normal minimum trigger current of 35mA, a suitable trigger current supplied by the current source I1 of the circuit of Figure 1 is typically 200 mA. In this case the duration of the pulse of trigger current  $I_G$  shown in Figure 2A is typically between 1  $\mu$ s and 2  $\mu$ s. The actual duration will firstly depend on the charge required to turn on the particular triac and will secondly depend on the speed with which the triac responds to that charge to turn on. The values of these two factors will vary from nominal values according to manufacturing variations for a nominally standard triac. The actual duration will thirdly depend on the time taken for the voltage across the triac  $V_T$  to drop below the value  $V_D$  from whatever value it is at when it starts to turn on, which will vary according to when the trigger pulse occurs within the half cycle of the source voltage  $V_s$ . By detecting the voltage across the triac  $V_T$  and terminating the trigger cur-

rent pulse when this voltage drops below the value  $V_D$ , the duration of the trigger current pulse is allowed to vary in response to these three varying factors.

5 Figure 2C shows the waveforms of Figure 2A at the time t4 on an expanded time scale. At the instant t40 the triac T is on such that the voltage  $V_T$  is substantially zero and the voltage  $V_L$  across the load is substantially  
10 that of the source voltage  $V_S$ . An interruption of the series connection of the triac and the load with the source voltage  $V_S$  reduces the voltage  $V_L$  and the voltage  $V_T$  to zero volts where they remain until the instant t41  
15 when the series connection is restored. The voltage  $V_T$  then rises towards the source voltage  $V_S$  while the voltage  $V_L$  remains substantially zero. At the instant t42 the voltage  $V_T$  becomes greater than the voltage  
20  $V_D$  and since this is during the period when the voltage  $V_C$  is still above the voltage  $V_R$ , the detector DET enables, via the gate G1, the comparator COMP to turn on the trigger current generator I1 to initiate a pulse of  
25 trigger current  $I_G$ . From the instant t42 to the instant t43 while trigger current  $I_G$  is supplied to the triac the triac remains off, the voltage  $V_T$  across it continues to rise towards the voltage  $V_S$  and the voltage across the load  $V_L$  remains  
30 substantially zero. At the instant t43 the triac begins to turn on, the voltage  $V_T$  begins to fall and the voltage  $V_L$  begins to rise. At the instant t44 the voltage  $V_T$  becomes less than the value  $V_D$  and so the comparator COMP is disabled  
35 by the gate G1 and turns off the trigger current generator I1 to terminate the pulse of trigger current  $I_G$ . At the instant t45 the triac has turned on, the voltage  $V_T$  is substantially zero, and the voltage across the load  $V_L$  is substantially the source voltage  
40  $V_S$ .

Referring now to Figure 3A, the control voltages  $V_C$  and  $V_R$ , pulses of trigger current  
45  $I_G$ , the voltage  $V_T$  across the triac and the voltage  $V_L$  across the resistive load are shown as waveforms on the same time scale as the source voltage  $V_S$  for the case in which the voltage  $V_C$  is continuously above  
50 the voltage  $V_R$ . In this case a pulse of trigger current  $I_G$  turns on the triac at the time t5, t6 and t7 very soon after the beginning of each half cycle of the alternating voltage  $V_S$ . At the times t5, t6 and t7 there is a  
55 temporary rise of the voltage  $V_T$  to just above the level at which the detection means DET is responsive, and the voltage  $V_L$  across the load is substantially the voltage  $V_S$  for substantially all the time. Figure 3B shows  
60 the waveforms of Figure 3A at the time t5 on an expanded time scale. At the instant t50 the voltage  $V_S$  reduces to zero which reduces the current through the triac T to zero and turns it off. The voltage  $V_T$  then rises  
65 substantially at the same value as the source

voltage  $V_S$  while the voltage across the load  $V_L$  is substantially zero volts. At the instant  
70 t51 the voltage  $V_T$  becomes greater than the voltage  $V_D$  and since the voltage  $V_C$  is above the voltage  $V_R$ , the detector DET enables, via the gate G1, the comparator COMP to turn on the trigger current generator I1 to  
75 initiate a pulse of trigger current  $I_G$ . From the instant t51 to the instant t52 while trigger current  $I_G$  is supplied to the triac the triac remains off, the voltage  $V_T$  across it continues to rise at substantially the voltage  
80  $V_S$  and the voltage across the load  $V_L$  remains substantially zero. At the instant t52 the triac begins to turn on, the voltage  $V_T$  begins to fall and the voltage  $V_L$  begins to rise. At the instant t53 the voltage  $V_T$  becomes  
85 less than the value  $V_D$  and so the comparator COMP is disabled by the gate G1 and turns off the trigger current generator I1 to terminate the pulse of trigger current  $I_G$ . At the instant t54 the triac has turned on, the voltage  $V_T$  is substantially  
90 zero, and the voltage across the load  $V_L$  is substantially the source voltage  $V_S$ .

The operation of the circuit of Figure 1 is illustrated for the case where the load L is inductive by the waveforms of Figure 4 and 5.

Referring to Figure 4A, the control voltages  $V_C$  and  $V_R$ , pulses of trigger current  
95  $I_G$  supplied by the current generator I1 to the triac T, the current  $I_{TL}$  through the triac T and the inductive load L, the voltage  $V_T$  across the triac T and the voltage  $V_L$  across the inductive load L are shown on the same  
100 scale as the voltage  $V_S$  of the alternating source. A pulse of trigger current  $I_G$  turns on the triac at the times t2, t4 and t5 which are at the beginning of the portion of each half cycle of the source voltage  $V_S$  for which  
105 the voltage  $V_C$  is above the voltage  $V_R$ . An extra pulse of trigger current  $I_G$  also occurs at the time t6 in response to a temporary interruption of the series connection of the triac and the load. Since the load L is inductive,  
110 the current  $I_{TL}$  through the triac T and the load L lags the voltage  $V_S$ . Thus at the time t0 when the voltage  $V_S$  is reduced to zero, current  $I_{TL}$  still flows through the triac and the load. The current  $I_{TL}$  reduces  
115 to zero at the time t1 so that the triac turns off, that is to say it goes into its high impedance condition such that the voltage  $V_T$  across the triac becomes substantially the voltage  $V_S$  whereas the voltage  $V_L$  across  
120 the load becomes substantially zero. The portion of the half cycle of the voltage  $V_S$  between the times t0 and t1 is the load phase angle. Between the times t1 and t2, the triac remains off and the voltages  $V_T$  and  $V_L$  remain  
125 substantially the same as the voltages  $V_S$  and zero volts respectively. At the time t2 the triac is turned on, the voltage  $V_T$  becomes substantially zero and the voltage  $V_L$  becomes  
130

becomes substantially the voltage  $V_s$ . The portion of the half cycle of the voltage  $V_s$  between the zero crossing of the voltage  $V_s$  at the time  $t_0$  and the pulse of trigger current at the time  $t_2$  is called the trigger angle. In the case shown in Figure 4A, the load phase angle is less than the trigger angle. Between the times  $t_2$  and  $t_3$  the voltage  $V_T$  remains substantially zero, the voltage  $V_L$  remains substantially the voltage  $V_s$  and a pulse of current  $I_{TL}$  is supplied from the source of voltage  $V_s$  to the load via the triac. A second pulse of current  $I_{TL}$  commences at the time  $t_4$  and a third pulse of current  $I_{TL}$  commences at the time  $t_5$ .

Figures 4B and 4C show the waveforms of Figure 4A at the times  $t_2$  and  $t_6$  on an expanded time scale. The operation of the circuit of Figure 1, and its effect on the waveforms  $I_G$ ,  $V_T$  and  $V_L$  at the instants  $t_{10}$  to  $t_{13}$  as shown in Figure 4B and at the instants  $t_{40}$  to  $t_{45}$  as shown in Figure 4C are the same as the operation of the circuit of Figure 1 and its effect on the waveforms  $I_G$ ,  $V_T$  and  $V_L$  which has already been described with reference to the instants  $t_{10}$  to  $t_{13}$  and the instants  $t_{40}$  to  $t_{45}$  shown in Figures 2B and 2C respectively. The effect on the waveform  $I_{TL}$  is also shown in Figures 4B and 4C and will be appreciated by comparison with the expanded waveforms of  $V_L$ .

Referring now to Figure 5A, the control voltages  $V_G$  and  $V_R$ , pulses of trigger current  $I_G$ , the current  $I_{TL}$  through the triac and the inductive load, the voltage  $V_T$  across the triac and the voltage  $V_L$  across the inductive load are shown as waveforms on the same time scale as the source voltage  $V_s$  for the case in which the voltage  $V_G$  is continuously above the voltage  $V_R$ . In this case a pulse of trigger current  $I_G$  turns on the triac at the times  $t_8$ ,  $t_9$  and  $t_{10}$  each time very shortly after the triac has turned off as a result of the reduction to zero of the current through the triac at the end of the load phase angle. The first zero crossing of the source voltage  $V_s$  on these waveforms is shown as occurring at the time  $t_7$ . The portion of the half cycle of the voltage  $V_s$  between the times  $t_7$  and  $t_8$  is the load phase angle. Since the voltage  $V_G$  is continuously above the voltage  $V_R$ , the trigger angle is zero. Thus in the case shown in Figure 5A the load phase angle is greater than the trigger angle. At the times  $t_8$ ,  $t_9$  and  $t_{10}$  there is a temporary rise of the voltage  $V_T$  to just above the level at which the detection means DET is responsive, and the voltage  $V_L$  across the load temporarily drops to zero volts. Otherwise the voltage  $V_L$  across the load is substantially the voltage  $V_s$  for substantially all the time, and the current  $I_{TL}$  through the triac and the load is substantially continuous. Figure 5B shows the waveforms of Figure 5A at the time  $t_8$  on an expanded time scale. At the

instant  $t_{80}$  the current  $I_{TL}$  reduces to zero and the triac turns off. From the instant  $t_{80}$  to the instant  $t_{82}$  the voltage across the load  $V_L$  drops from substantially the source voltage  $V_s$  to substantially zero volts. From the instant  $t_{80}$  the voltage across the triac  $V_T$  rises towards the source voltage  $V_s$ . At the instant  $t_{81}$  the voltage  $V_T$  becomes greater than the voltage  $V_D$  and, since the voltage  $V_G$  is above the voltage  $V_R$ , the detector DET enables, via the gate G1, the comparator COMP to turn on the trigger current generator I1 to initiate a pulse of trigger current  $I_G$ . From the instant  $t_{81}$  to the instant  $t_{83}$  while trigger current  $I_G$  is supplied to the triac the triac remains off, so that the current  $I_{TL}$  remains zero and the voltage  $V_T$  across the triac continues to rise towards the voltage  $V_s$ . The voltage across the load  $V_L$  remains substantially zero from the instant  $t_{82}$  to the instant  $t_{83}$ . At the instant  $t_{83}$  the triac begins to turn on, the current  $I_{TL}$  begins to rise, the voltage  $V_T$  begins to fall and the voltage  $V_L$  begins to rise. At the instant  $t_{84}$  the voltage  $V_T$  becomes less than the value  $V_D$  and so the comparator COMP is disabled by the gate G1 and turns off the trigger current generator to terminate the pulse of trigger current  $I_G$ . At the instant  $t_{85}$  the triac has turned on, the current  $I_{TL}$  is on the curve of the substantially continuous current pulse shown in Figure 5A, the voltage  $V_T$  is substantially zero and the voltage across the load  $V_L$  is substantially the source voltage  $V_s$ .

The operation of the circuit of Figure 1 for the case where the load L is capacitive will be similar to the operation just described with reference to Figures 4 and 5, taking into account the fact that the current  $I_{TL}$  will lead the voltage  $V_s$  instead of lagging it.

Possible realisations of the component parts of the circuit shown in Figure 1 will now be described in detail.

Referring to Figures 6 and 7, the ramp waveform generator 100 and its operation are shown in detail. The base and emitter respectively of two transistors TR1 and TR2 are respectively connected to the junction of two resistors R1 and R2 connected between the line terminal 2 which is at the alternating source voltage  $V_s$  and the neutral terminal 1 which is at zero volts. The emitter and base respectively of the transistors TR1 and TR2 are connected to the neutral terminal 1 of the alternating voltage source, and the collectors of both transistors TR1 and TR2 are connected via a current source I2 to the rectified negative voltage supply  $-V$ . The collectors of the transistors TR1 and TR2 are also connected to the base of a transistor TR3 whose emitter is connected to the zero voltage terminal 1 and whose collector is connected via a resistor R3 to the negative voltage supply  $-V$ . A capacitor

$C_R$  is connected between the zero voltage terminal 1 and the collector of the transistor TR3.

When the alternating voltage  $V_s$  is low, that is to say close to zero volts, then the transistors TR1 and TR2 both do not conduct and so the current source I2 can switch on the transistors TR3. The periods during which the transistor TR3 is switched on are shown by the lower level portions of the pulse voltage waveform A; and during these periods the transistor TR3 discharges the capacitor  $C_R$  towards the zero voltage terminal 1 which is shown by the rising portion of the ramp voltage waveform  $V_R$ . During each half cycle of the alternating source voltage when the voltage  $V_s$  at the terminal 2 is sufficiently positive or sufficiently negative, then the transistor TR2 or the transistor TR1 respectively will conduct and the transistor TR3 will be switched off. The capacitor  $C_R$  will during this time charge via the resistor R3 towards the negative voltage supply  $-V$  which is shown by the falling portion of the ramp voltage waveform  $V_R$ .

The voltage comparator COMP shown in Figure 1 which compares the d.c. control voltage  $V_C$  and the ramp voltage waveform  $V_R$  may be realised as shown in Figure 8. A long tailed pair of transistors TR4 and TR5 is operative to compare the voltages  $V_C$  and  $V_R$  applied to their respective bases when a current source I3 connected between their two emitters and the zero voltage neutral terminal 1 is gated on by the output of the NAND gate G1. When the ramp voltage  $V_R$  is lower than the control voltage  $V_C$  the transistor TR4 conducts and the transistor TR5 does not conduct and vice versa. The collectors of the transistors TR4 and TR5 are connected to the collector and base respectively of a transistor TR6 whose emitter is connected to the negative voltage supply  $-V$ . When the transistor TR4 conducts and the transistor TR5 does not conduct, then the transistor TR6 conducts and the potential across the transistor TR6 turns on the trigger current generator I1. When the transistor TR5 conducts and TR4 does not conduct then TR6 will prevent any input into I1, interference resulting from leakage currents thus being prevented. When the current source I3 is not gated on by the output of the gate G1, both transistors TR4 and TR5 cannot conduct and therefore the trigger current generator I1 cannot be turned on.

The detection means DET shown in Figure 1 which is responsive to the voltage across the triac T may be realised as shown in Figure 9. A potential divider consisting of resistors R4 and R5 is connected between the zero volts neutral terminal 1 and the anode of the triac T. This reduces the mag-

nitude of the voltage  $V_T$  across the triac T to an appropriate level at the junction of the resistors R4 and R5 which junction is connected to the emitter of a transistor TR7 and the base of a transistor TR8. The base of the transistor TR7 and the emitter of the transistor TR8 are connected to the terminal 1. The collectors of the transistors TR7 and TR8 are connected together and, via the resistor R6, to the negative voltage supply  $-V$ . The collectors of the transistors TR7 and TR8 also provide an output to the NAND gate G1. When the voltage  $V_T$  across the triac T is of positive polarity or of negative polarity having a magnitude greater than the voltage  $V_D$  then the transistor TR7 or the transistor TR8 respectively conducts and provides the first detection signal to the NAND gate G1. If the NAND gate G1 is enabled by the output signal of the supply circuit 200, this first detection signal enables the comparator COMP. When the voltage  $V_T$  across the triac T is of positive polarity or of negative polarity having a magnitude less than the voltage  $V_D$  then the transistors TR7 and TR8 both do not conduct and the second detection signal is provided to the NAND gate G1 whereby the comparator COMP is disabled.

The supply circuit 200 shown in Figure 1 which provides the negative voltage supply  $-V$  from the alternating voltage source and also an output signal if the magnitude of the supply  $-V$  is less than a predetermined value may be realised as shown in Figure 10. A possible realisation of the trigger current generator I1 which is part of the circuit shown in Figure 1 is also shown in Figure 10. The alternating source voltage across the neutral terminal 1 and the line terminal 2 is rectified by a half-wave rectifying diode D1, lowered in voltage by a resistor R7 and smoothed by an electrolytic capacitor  $C_s$ . The voltage across the capacitor  $C_s$  provides the negative supply voltage  $-V$  and this is stabilised at a typical value of  $-8$  volts by two diodes D2 and D3 and a zener diode Z connected in series with each other and in parallel with the capacitor  $C_s$ . The trigger current generator I1 consists of a transistor TR9 whose emitter is connected to the supply  $-V$ , whose collector is connected to the gate electrode of the triac T via a resistor R8 and whose base is connected to the output of the comparator COMP.

When the transistor TR9 is turned on by the output of the comparator COMP it supplies a current to the gate electrode of the triac T whose value is determined by the resistor R8. As has been previously mentioned, a typical trigger current pulse supplied by the source I1 has an amplitude of 200 mA but a short duration of  $2 \mu s$  or less. Furthermore, as has been explained above with reference to Figures 2 to 5, in normal



operation of the circuit a trigger current pulse occurs only once per half cycle of the alternating voltage source. Since the high trigger current of 200 mA is required for such a small proportion of each half cycle of the alternating voltage source, the total averaged continuous current consumption of all the component parts of the circuit of Figure 1 which are supplied with the negative voltage supply  $-V$  from the supply circuit 200 is low. This means that the electrolytic capacitor  $C_s$  of the supply circuit 200 discharges by only a small amount during alternate half cycles of the source voltage, and a small charging current to the capacitor  $C_s$  of typically 5 mA r.m.s. supplied through a high value resistor  $R7$  of typically 50K ohms in the other alternate half cycles of the source voltage is ample to maintain the supply voltage  $-V$  at its required value of typically  $-8$  volts. The resulting low power dissipation of the resistor  $R9$ , typically 0.6 watts, is of course also advantageous for the cool running of the circuit.

A transistor  $TR10$  has its emitter connected to the neutral line 1, its base is connected via a resistor  $R9$  to the junction of the diode  $D3$  and the zener diode  $Z$ , and its collector is connected via a resistor  $R10$  to the supply voltage  $-V$ . The collector of the transistor  $TR10$  provides an output to the NAND gate  $G1$ . The transistor  $TR10$  will conduct and provide an enabling signal to the gate  $G1$  if the voltage across the capacitor  $C_s$  is greater than the zener voltage of zener diode  $Z$  and the diode voltage of the diode  $D3$ , typically 7.3 volts for a nominal stabilised voltage of  $-8$  volts of the supply  $-V$ . If the voltage across the capacitor  $C_s$  is less than this value of 7.3 volts then the gate  $G1$  is disabled and the trigger current generator  $I1$  cannot be turned on. With the power supply circuit 200 realised in the manner described, this enabling output to the gate  $G1$  is necessary to ensure that the trigger current generator  $I1$  can only be turned on when the supply  $-V$  is large enough for it to supply a trigger current whose amplitude is sufficient to turn on the triac  $T$ .

Some possible modifications with the scope of the invention of the detailed embodiment described above with reference to Figures 1 to 10 are as follows.

In the above-described circuit of Figure 1 the trigger current generator  $I1$  provides a negative trigger current to the gate electrode of the triac  $T$  which turns it on in both the positive polarity and negative polarity half cycles of the alternating source voltage. The trigger current generator could be adapted to provide a positive trigger current instead. Another possibility is to provide a trigger current generator which produces negative trigger current and positive trigger current to

the gate electrode of the triac  $T$  in alternate half cycles of the alternating voltage source.

In the above-described circuit of Figure 1 a variable d.c. control voltage  $V_G$  and a fixed ramp waveform voltage  $V_R$  are applied to the comparator  $COMP$ . Alternatively, the d.c. control voltage  $V_G$  could be fixed and the ramp waveform voltage  $V_R$  could be variable. This is to say that the frequency of the ramp waveform  $V_R$  would remain fixed at double the frequency of the alternating voltage source but the waveform of that frequency could be variable so as to control the point in each half cycle at which the voltage  $V_R$  goes below the voltage  $V_G$ . For this purpose a variable resistor or a variable capacitor could be used to vary the shape of the waveform  $V_R$ , or a variable potential could be used to vary the level of a fixed shape waveform  $V_R$ .

In the above description, Figures 3 and 5 illustrate the operation of the circuit of Figure 1 when the voltage  $V_G$  is continuously above the voltage  $V_R$ . With the frequency of the waveform  $V_R$  supplied by the ramp waveform generator 100 at double the frequency of the alternating voltage source, Figures 3 and 5 show the full firing condition, that is to say substantially continuous current supply to the load, for phase (conductive angle) control of the triac  $T$ . It will be appreciated that by the simple means of modifying the ramp waveform generator 100 to provide a voltage waveform  $V_R$  having a lower frequency, for example one thousandth that of the alternating source voltage, the circuit of Figure 1 will provide burst firing (time proportional) control of the triac  $T$ . In this case the voltage  $V_G$  will be above the voltage  $V_R$  for a number of half cycles of the alternating voltage source which is a proportion of the number of half cycles in each period of the waveform  $V_R$ , and for that proportion of each period of the waveform  $V_R$  trigger pulses will occur once per half cycle in the same manner as shown in Figures 3 and 5 to maintain a substantially continuous current supply to the load  $L$ .

A further possibility is to provide a variable d.c. voltage instead of a ramp waveform  $V_R$ , for example a temperature dependent d.c. voltage which is compared with the control voltage  $V_G$  to provide thermostatic control of current to the load  $L$  in the form of a heating resistor. This is an example of static (on-off) control of the triac  $T$ , that is to say that substantially continuous current will be supplied to the load  $L$  in the manner shown in Figure 3 while the voltage  $V_G$  is above the temperature dependent voltage substituted for the ramp voltage  $V_R$  and no current will be supplied to the load while the voltage  $V_G$  is below that temperature dependent voltage. Static control for inductive or capacitive loads may also be provided



with continuous current supply during the "on" periods in the manner shown in Figure 5.

The detection means DET of the circuit of Figure 1 which is shown in detail in Figure 9 is arranged to provide a first detection signal if the voltage across the triac T is greater than a first predetermined value, and to provide a second detection signal if the voltage across the triac T is smaller than a second predetermined value. The first and second predetermined values coincide at the value  $V_D$  which is typically 20 volts. However, the first and second predetermined values fulfill different criteria and so need not be coincident. The detection means DET could be suitably realised in a manner different to that shown in Figure 9 so as to respond to first and second predetermined values of the voltage across the triac which are not coincident.

In the circuit shown in Figure 1, the detection means DET, comparator COMP and the trigger current generator 11 are connected in the circuit such that the first and second detection signals respectively enable and disable the comparator COMP and such that the output of the comparator COMP turns the trigger current generator 11 on and off. However, the comparator COMP could be permanently enabled and its output gated with the output of the detection means DET via a suitably rearranged gate G1 to turn the trigger current generator 11 on and off. In either case, means are provided interconnecting the comparator COMP and the detection means DET such that, in normal operation, during those periods of time when a first control voltage applied to the comparator COMP is above a second control voltage applied to the comparator COMP, control means including the comparator COMP, the detection means DET and the interconnection means is responsive to the first and second detection signals to respectively turn on and turn off the trigger current generator 11.

The circuit shown in Figure 1 includes a triac T via which current can be supplied to the load L in both half cycles of the alternating source voltage. Another example of a semiconductor switch which can be used in a circuit according to the invention is a thyristor. The detailed circuit of Figure 1 would be modified as follows. A positive rectified supply voltage would be provided instead of the negative rectified supply  $-V$ . The detection means DET would be re-arranged to respond to voltage across the thyristor of only one polarity. The trigger current generator 11 would be such as to supply positive trigger current to the gate electrode of the thyristor. The thyristor can be in series with the load and the alternating voltage source via a bridge rectifier, or the thyristor can be

one of a pair of thyristors included in a bridge rectifier each thyristor being thereby in series with the load and the alternating voltage source. Alternatively the thyristor can be used to supply current to the load only in half cycles of the alternating voltage source of a single polarity. In this latter case, when the circuit is used for phase control, the ramp voltage waveform generator 100 shown in detail in Figure 6 would be re-arranged so that the capacitor  $C_R$  remains discharged for alternate half cycles of the alternating voltage source.

#### WHAT WE CLAIM IS:—

1. A circuit for supplying electrical current from an alternating voltage source to a load, including a semiconductor switch for connection in series with the load such that current is supplied to the load via the switch while the switch is on, a trigger current generator for supplying trigger current to the switch to turn on the switch, and control means for turning on and off the trigger current generator, characterised in that the control means includes comparator means for comparing two control voltages, detection means responsive to the voltage across the switch, said detection means being adapted to provide a first detection signal if the voltage across the switch is larger in amplitude than a first predetermined value which is near zero volts but large enough such that if the switch is off it will hold on if it is then turned on, said detection means also being adapted to provide a second detection signal if the voltage across the switch is smaller in amplitude than a second predetermined value which is also near zero volts and furthermore is small enough to indicate that the switch has been substantially turned on when it had previously been off, and means interconnecting the comparator means and the detection means such that, in normal operation, during those periods of time when a first one of said control voltages is above a second one of said control voltages the control means is responsive to the first and second detection signals to respectively turn on and turn off the trigger current generator.

2. A circuit as claimed in Claim 1, in which said first and second predetermined values coincide.

3. A circuit as claimed in Claim 1 or Claim 2, in which the semiconductor switch is a triac, in which one of the two control voltages is a variable d.c. reference voltage and in which means are provided for producing the other of the two control voltages as a ramp waveform at double the frequency of the alternating voltage source, whereby for a given value of the d.c. reference volt-

age the first one of said control voltages is above the second one of said control voltages for a given portion of each half cycle of the alternating voltage source.

- 5 4. A circuit as claimed in any one of Claims 1 to 3, in which the detection means, comparator means and trigger current generator are connected in the circuit such that the first and second detection signals respectively enable and disable the comparator means and such that the output of the com-
- 10

parator means turns the trigger current generator on and off.

5. A circuit for supplying electrical current from an alternating voltage source to a load substantially as herein described with reference to the accompanying drawings. 15

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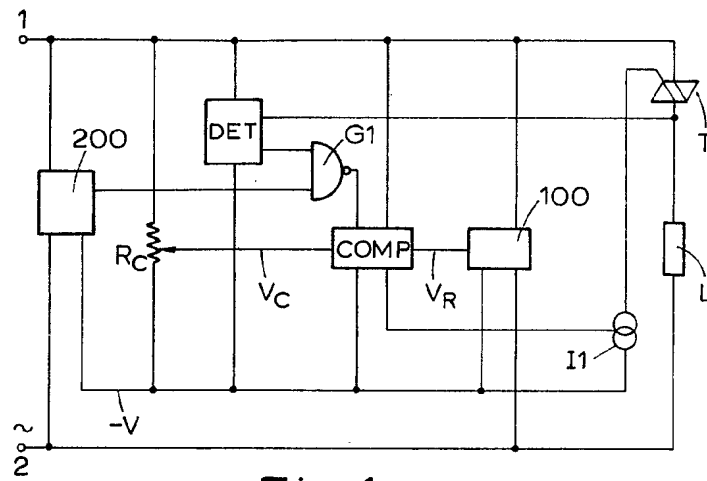


Fig.1

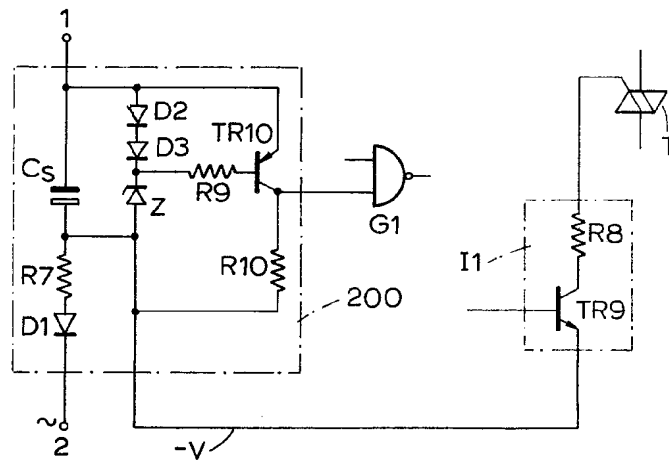


Fig.10

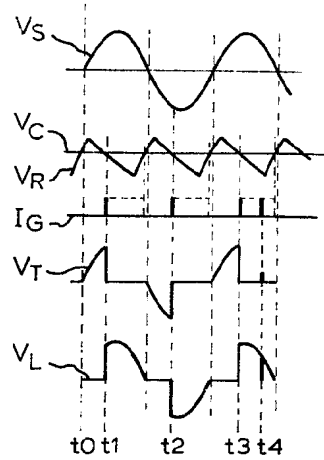


Fig. 2A

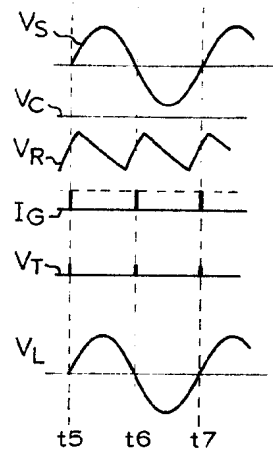


Fig. 3A

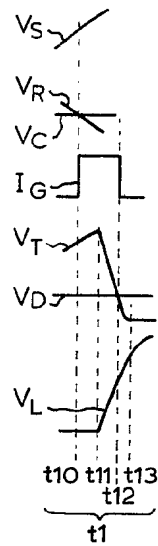


Fig. 2B

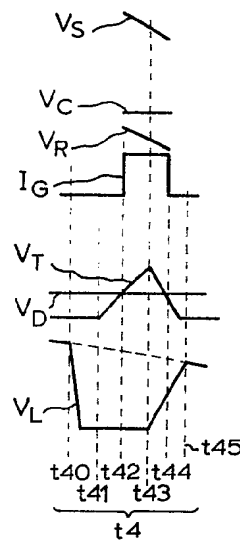


Fig. 2C

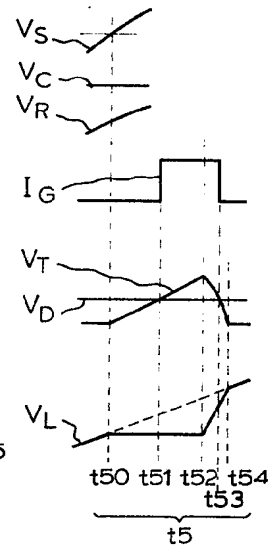
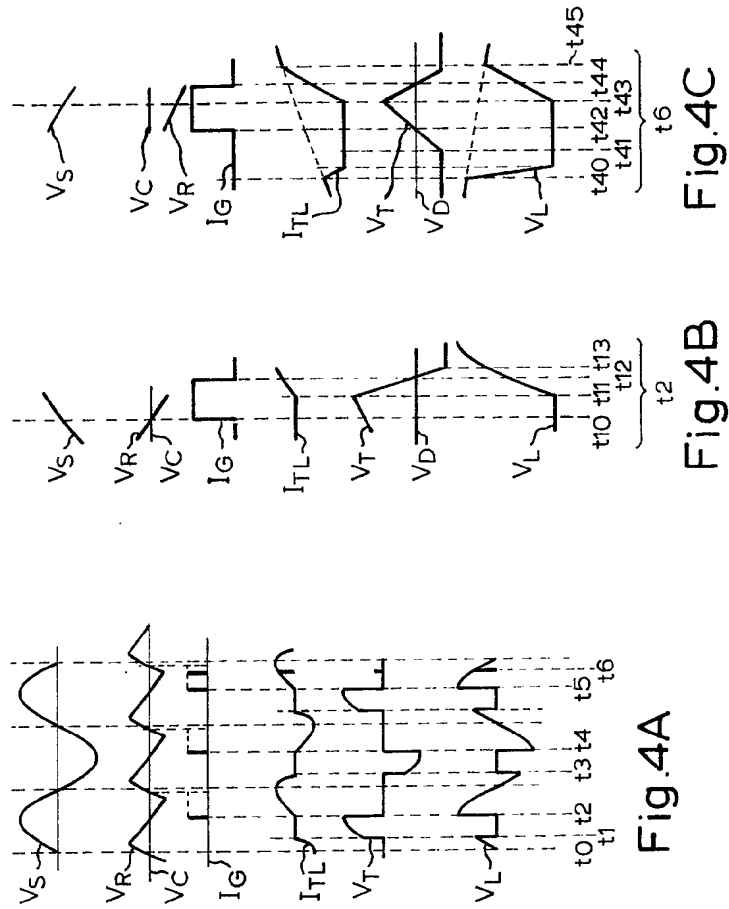
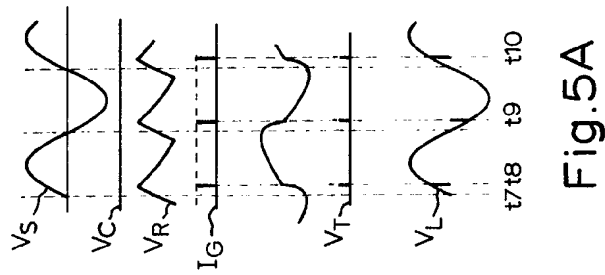
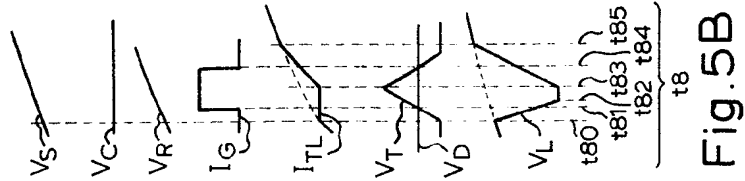


Fig. 3B





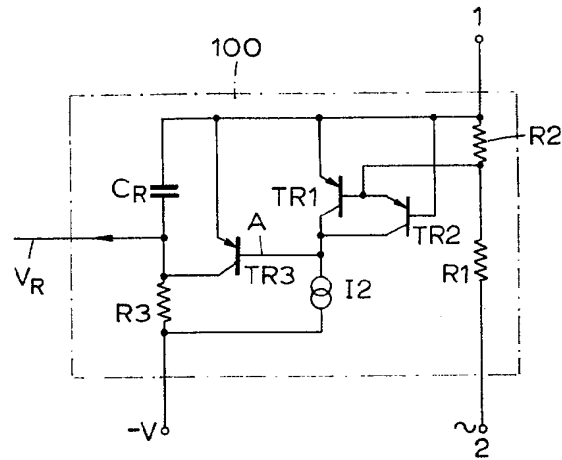


Fig. 6

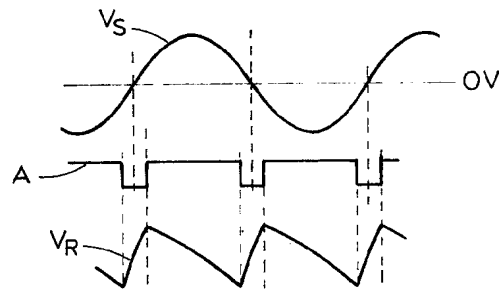


Fig. 7



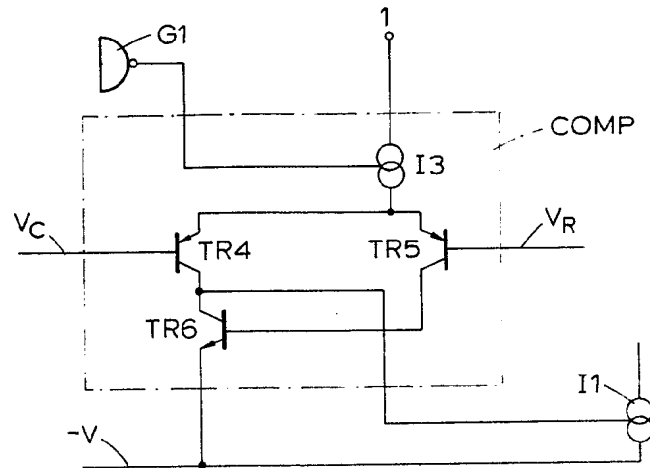


Fig. 8

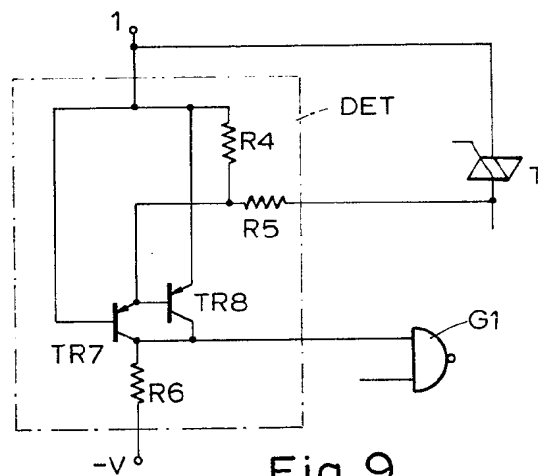


Fig.9